SURFACE PASSIVATION OF ATMOSPHERIC PRESSURE DRY ETCHED MULTICRYSTALLINE SILICON SURFACES

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ABSTRACT: In this work, we investigate the electrical performance of multicrystalline silicon (mc-Si) solar cell precursors in terms of minority charge carrier lifetime and implied open-circuit voltage as a function of the different surface passivation layers applied. Here, we applied a plasma-less nanotexturing process by atmospheric pressure dry etching (ADE) that enables low reflectivity, followed by a short anisotropic alkaline etch. It is seen that surface reflection and carrier lifetime both exhibit dependency on surface morphology of nanostructures and such dependency can be affected by variations adapted in surface passivation. It is also seen in our investigation that on the front surface additional surface passivation layer applied by fast atomic layer deposition (ALD) of Al_2O_3 followed by plasma-enhanced chemical vapor deposition (PECVD) of SiN_x as standard anti-reflection coating (ARC) shows relatively higher implied open-circuit voltage than implied open-circuit voltage gained by standard ARC layer of PECVD-SiN_x.

Keywords: Atmospheric pressure dry etch (ADE), nanotexture, multicrystalline silicon, surface passivation

1 INTRODUCTION

Alternatives to the current industry standard wet-chemical texturing methods for multicrystalline silicon (mc-Si) have been extensively investigated by the photovoltaic community already for long now [1–5]. In recent times, nanotexturing processes or black silicon (B-Si) have generated new interest due to their competence to reach low reflectivity and higher solar cell efficiencies than state-of-the-art wet-chemical texture on diamond-wire sawn mc-Si wafers. Recently, the atmospheric pressure dry etching (ADE) process has demonstrated efficiencies above 20% [6, 7] on diamond-wire sawn (DWS) mc-Si passivated emitter and rear cell (PERC) type architecture. This universal texturing process is also applicable to monocrystalline silicon (c-Si) wafers as well as for other novel wafering techniques such as kerfless wafering [8, 9].

As a continuous step towards the integration of plasma-less ADE technique in solar cell processing, we investigate the performance of fast atomic layer deposition (ALD) of dielectric material aluminium oxide (Al_2O_3) as a surface passivating layer in comparison to silicon nitride (SiN_x) prepared by plasma-enhanced chemical vapor deposition (PECVD) on mc-Si substrates. The surfaces are textured by applying ADE texture that enables low reflectivity. The texturing process is followed by a short wet etch prior to the passivation layer deposition. We investigate the surface passivation for different emitter diffusion processes in terms of implied open-circuit voltage (iV_{oc}), weighted surface reflection (R_w) and lifetime of minority charge carriers (τ_{PL}). The investigation allows further optimization of the ADE texture and the subsequent cell manufacturing processing steps to achieve higher conversion efficiencies.

2 APPROACH

2.1 Experiment design

The process workflow is presented in Figure 1. All the groups used boron-doped *p*-type mc-Si wafers as precursors (≈ 1.6 Ωcm base resistivity).

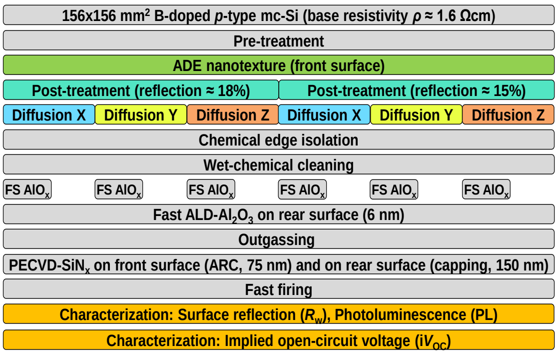


Figure 1: Schematic diagram of process workflow (FS indicates front surface).

The surface areas of 156x156 mm^2 each were saw-damage etched using an anisotropic alkaline process. The samples were then processed in the inline atmospheric pressure dry etching (ADE) tool [9] to create rough B-Si structures. In order to decrease surface roughness, the wafers subsequently went through another short anisotropic alkaline process, which was adjusted to reach two different average values of surface reflections at the wavelength of 600 nm ($R_{600} \approx 18\%$ and $R_{600} \approx 15\%$).

Three different emitters (diffusion X, Y, Z) were diffused in each post-treated ADE group by industry-type $POCl_3$-based tube diffusion furnace, followed by chemical edge isolation including phosphosilicate glass (PSG) etching. Diffusion X [10] applied an increased in-situ oxidation process, whereas diffusion Y used shorter and diffusion Z used longer total process time compared to diffusion X. Each diffused group was then divided into two sub-groups – one sub-group received fast ALD-Al_2O_3 passivation on front surface (2 nm) and other sub-group without any Al_2O_3 passivation on front surface; although both of these sub-groups received ALD-Al_2O_3 passivation on rear surface (6 nm).

Afterward, all groups were annealed at a low-temperature so-called “outgassing” process [11] and then received final coating by applying plasma-enhanced chemical vapor deposition (PECVD) SiN_x (75 nm on front surface as anti-reflection coating (ARC) and 150 nm on rear surface as capping-layer). After surface passivation, all groups were fired at a set temperature of 850 °C.

The precursors went through all process steps typically applied to fabricate PERC architecture apart from metallization and finally were subjected to implied open-circuit voltage (iV_{oc}) characterization using quasi-steady state photoconductance (QSSPC) measurements [12], AM 1.5 weighted surface reflection (R_w) and lifetime-calibrated photoluminescence (PL) measurements.

2.2 Characterization

Wafers from the two different reflection groups ($R_{600} \approx 18\%$ and 15%) and the three different emitters (diffusion X, Y, Z) were selected from both passivation variations on front surface (fast ALD-Al_2O_3/PECVD-SiN_x stacks vs. only PECVD-SiN_x) for investigating lifetimes of minority charge carriers for arbitrary surface co-ordinates from lifetime-calibrated PL imaging to investigate the correlation of the carrier lifetime (τ_{PL}) and the weighted surface reflection (R_w) measured for the spectrum of 280–1200 nm for respective surface co-ordinates [13].

Later all samples were characterized for implied open-circuit voltage by applying QSSPC technique, where each sample was subjected to five QSSPC measurements.

Apart from electrical characterization, ADE textured wafers were investigated by scanning electron microscopy (SEM) for investigating the surface morphology and textured structures for un-passivated and for passivated samples.

3 RESULTS AND DISCUSSION

3.1 ADE-textured surface morphology

Nanoscale features of ADE textured surface represent potential challenges in terms of surface passivation. In contrary to standard-textured surfaces passivated with SiN_x, a conformal surface passivating layer cannot be fully delivered by the PECVD technique alone, especially for nanotextured structures. ADE-textured surface presents areas relatively difficult to passivate conformally by PECVD-SiN_x passivation [14]. Hence, an additional passivating layer of Al_2O_3 was applied before passivating with SiN_x deposition. Figure 2 presents SEM image of such surface passivation.

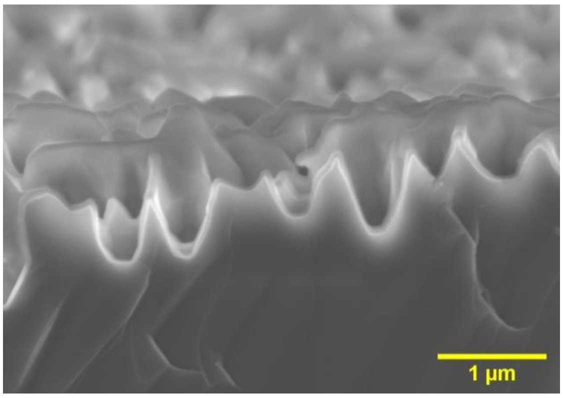
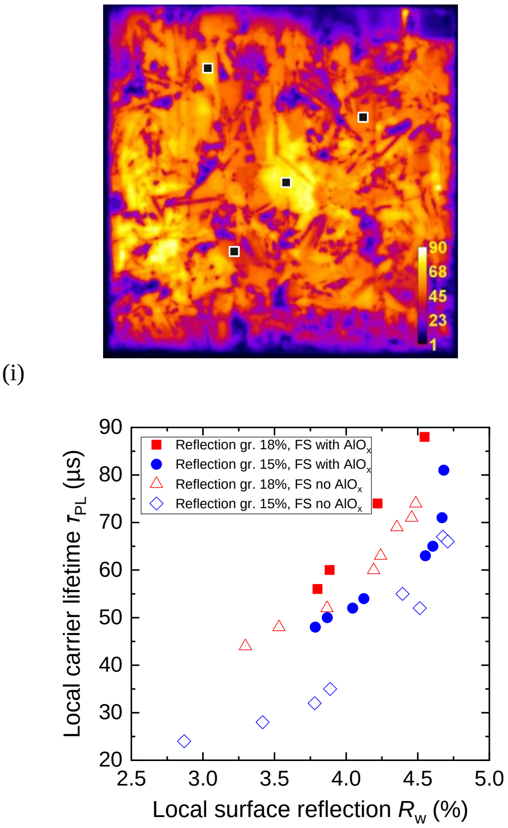


Figure 2: SEM cross-section image of ADE textured surface passivated with fast ALD-Al_2O_3/PECVD-SiN_x stacks.

The conformal layer of Al_2O_3 was applied by using fast atomic layer deposition (ALD); whereas the SiN_x layer was prepared by plasma-enhanced chemical vapor deposition (PECVD) on the ADE textured mc-Si wafer substrates.

3.3 Correlation between carrier lifetime and surface reflection

Figure 4(i) shows few arbitrary measurement points on a lifetime-calibrated PL image applied for locally comparing carrier lifetime and weighted surface reflection. Figure 4(ii) shows locally the dependency of minority charge carrier lifetimes (τ_{PL}) corresponding to different local (R_w) surface reflections along the wafer surface for ADE-textured wafers as comparison between surface passivation with stacks of fast ALD-Al_2O_3/PECVD-SiN_x versus only PECVD-SiN_x for both reflection groups ($R_{600} \approx 18\%$ and $R_{600} \approx 15\%$).



(i)

(ii)

Figure 4: (i) Lifetime-calibrated photoluminescence (PL) image of an exemplary wafer surface indicating few arbitrary points on the surface where the correlation between minority charge carrier lifetime (τ_{PL}) and local surface reflection (R_w) was investigated. (ii) Correlation between τ_{PL} and R_w of passivated ADE textured surface.

The lifetime of the minority charge carriers are obtained by lifetime-calibrated PL images. Each symbol in the graph represents one measurement at one spot. It seems that samples passivated with fast ALD-Al_2O_3 on front surface exhibit potentially higher carrier lifetimes compared to the samples without an Al_2O_3 layer on front.

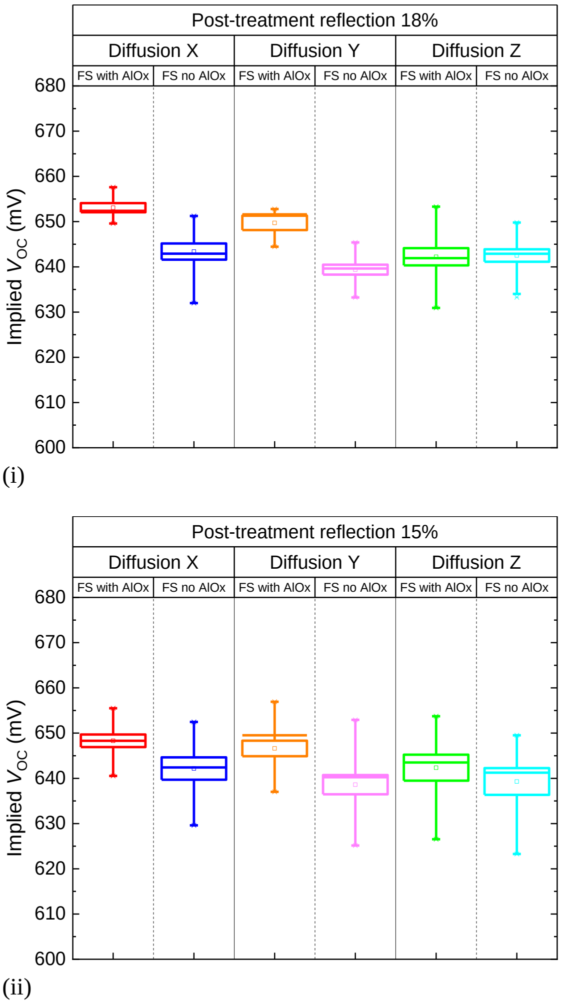
This behavior was expected to be related to the conformality of Al_2O_3 layer that contributes to the enhancement of the surface passivation, and was observed in both reflection groups of $R_{600} \approx 18\%$

and R_{600} ≈ 15% that is in consistency with the literature [5–9] [15–17].

Within the measured range, it is found that the carrier lifetime scales with the weighted surface reflection. Surfaces exhibiting a more rough morphology are beneficial for low R_w but decrease τ_{PL}.

3.2 Implied open-circuit voltage (iV_{oc})

A conformal layer of ALD-Al_2O_3 passivates the nanotexture as such that it results in a lower surface recombination value leading to less surface recombination, hence potentially higher iV_{oc} can be obtained. Thus, groups having Al_2O_3 on the front surface feature a potentially higher iV_{oc} than groups without Al_2O_3 on front, independent of the reflection groups for surface modification (R_{600} ≈ 18% and R_{600} ≈ 15%) and the diffused emitters (diffusion X, Y, Z), as apparent from Figure 5.



(i)

(ii)

Figure 5: Implied open-circuit voltage (iV_{oc}) values at 1-sun illumination extracted from the QSSPC-measured lifetime data.

It was seen that for all groups with an Al_2O_3 passivated front surface, the mean iV_{oc} reaches 647 mV with a maximum iV_{oc} value reaching 658 mV for the nanotextured surface with 18% reflection and diffusion X. On the other hand, for all groups without Al_2O_3 on front surface, the mean iV_{oc} reaches 641 mV with a maximum iV_{oc} value reaching 653 mV.

4 CONCLUSION

Conventionally deposited PECVD-SiN_x layer remains mostly on the upper section of the ADE texture geometry, thus the valleys of the nanostructures remain partly un-passivated, whereas thin ALD-Al_2O_3 forms very conformal layer in the nanostructure [5–8]. Such characteristic of ALD-deposited layers in comparison to the PECVD-deposited layers have also been reported by others, especially, on rough surfaces like B-Si structures for excellent conformity, leading to reasonably low surface recombination velocities [13–15].

In this experiment, higher degree of surface passivation using fast ALD-Al_2O_3 is availed in each reflection group due to its conformality. It is also seen that such conformality of Al_2O_3 is persistent for all nanotexture groups that receive further variations in the emitter diffusion process. It represents a potential gain in iV_{oc} of up to 5 mV, if the wafers are passivated with fast ALD-Al_2O_3 on front surface despite an already smoothened surface morphology obtained by the post-etching process performed just after ADE texturing.

Since nanotextures result in smaller features, high aspect ratios and increased surface roughness, the emitter formation and the surface passivation are potentially affected while drawing an impact on solar cell performances. This investigation allows us to understand implications of the emitter formation and the subsequent surface passivation on the implied open-circuit voltages that are achievable on ADE textured mc-Si surfaces. Our study shows and discusses these implications on an experimental basis, which may play a significant role to further optimize emitter formation and surface passivation of nanotextured mc-Si.

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